BT232-800D

4Q Triac

Rev.02 - 09 January 2025 Product data sheet

1. General description

Planar passivated very sensitive gate four quadrant triac in a TO92 plastic package intended for use in applications requiring direct interfacing to logic ICs and low power gate drivers.

2. Features and benefits

- High blocking voltage capability
- Very sensitive gate
- Planar passivated for voltage ruggedness and reliability
- Triggering in all four quadrants
- Direct interfacing to logic level ICs
- Direct interfacing to low power gate drive circuits

3. Applications

- Industrial process control
- General purpose low power motor control
- Home appliances
- Low power AC Fan controllers

4. Quick reference data

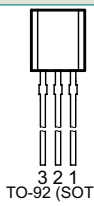
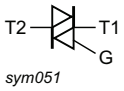
Table 1. Quick reference data

Symbol	Parameter	Conditions	Notes	Values			Unit
Absolute maximum rating							
V_{DRM}	repetitive peak off-state voltage			800			V
$I_{T(RMS)}$	RMS on-state current	full sine wave; Fig. 1; Fig. 2		2			A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)}$ = 25 °C; t_p = 20 ms; Fig. 3; Fig. 4		16			A
		full sine wave; $T_{j(init)}$ = 25 °C; t_p = 16.7 ms		17.5			A
T_j	operating junction temperature			-40 to 125			°C
Symbol	**Parameter**	**Conditions**	**Notes**	**Min**	**Typ**	**Max**	**Unit**
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T2+ G+; T_j = 25 °C; Fig. 6		-	-	5	mA
		V_D = 12 V; I_T = 0.1 A; T2+ G-; T_j = 25 °C; Fig. 6		-	-	5	mA
		V_D = 12 V; I_T = 0.1 A; T2- G-; T_j = 25 °C; Fig. 6		-	-	5	mA
		V_D = 12 V; I_T = 0.1 A; T2- G+; T_j = 25 °C; Fig. 6		-	-	10	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 8		-	-	10	mA
V_T	on-state voltage	I_T = 2 A; T_j = 25 °C; Fig. 9		-	1.35	1.65	V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 110 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 11		20	-	-	V/µs
dV_{com}/dt	rate of change of commutating voltage	V_D = 400 V; T_j = 110 °C; dI_{com}/dt = 0.44 A/ms; I_T = 1 A; gate open circuit		1	-	-	V/µs

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T2	main terminal 2	 TO-92 (SOT54)	 *sym051*
2	G	gate		
3	T1	main terminal 1		

6. Ordering information

Table 3. Ordering information

Type number	Package Name	Orderable part number	Packing method	Small packing quantity	Package version	Package issue date
BT232-800D	TO92	BT232-800D,412	Bulk	1000	TO92L	10-May-2021

7. Marking

Table 4. Marking codes

Type number	Marking codes
BT232-800D	232-8D

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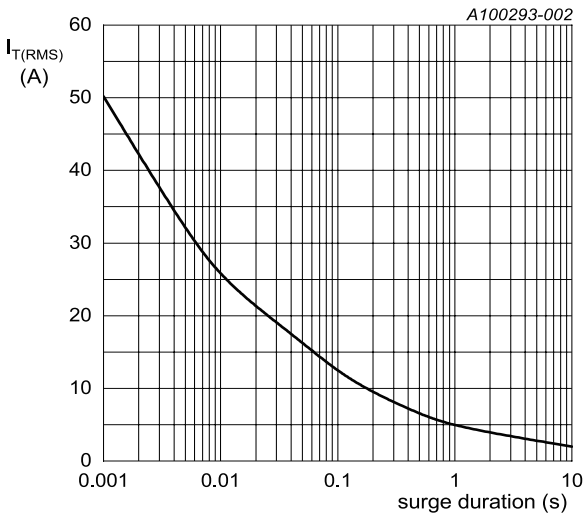
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Notes	Values	Unit
V_{DRM}	repetitive peak off-state voltage			800	V
V_{RRM}	repetitive peak reverse voltage			800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; Fig. 1; Fig. 2		2	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)}$ = 25 °C; t_p = 20 ms; Fig. 3; Fig. 4		16	A
		full sine wave; $T_{j(init)}$ = 25 °C; t_p = 16.7 ms		17.5	A
I^2t	I^2t for fusing	t_p = 10 ms; SIN		1.28	A^2s
dI_T/dt	rate of rise of on-state current	I_G = 20 mA		50	A/µs
I_{GM}	peak gate current			1	A
P_{GM}	peak gate power			2	W
$P_{G(AV)}$	average gate power	over any 20 ms period		0.1	W
T_{stg}	storage temperature			-40 to 150	°C
T_j	operating junction temperature			-40 to 125	°C



f = 50 Hz

Fig. 1. RMS on-state current as a function of surge duration; maximum values

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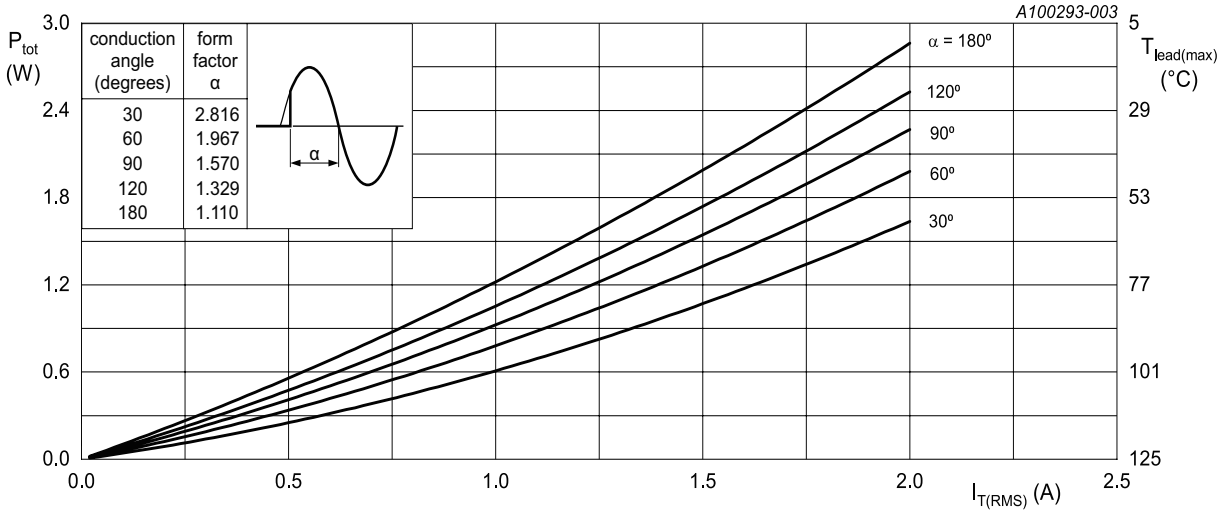
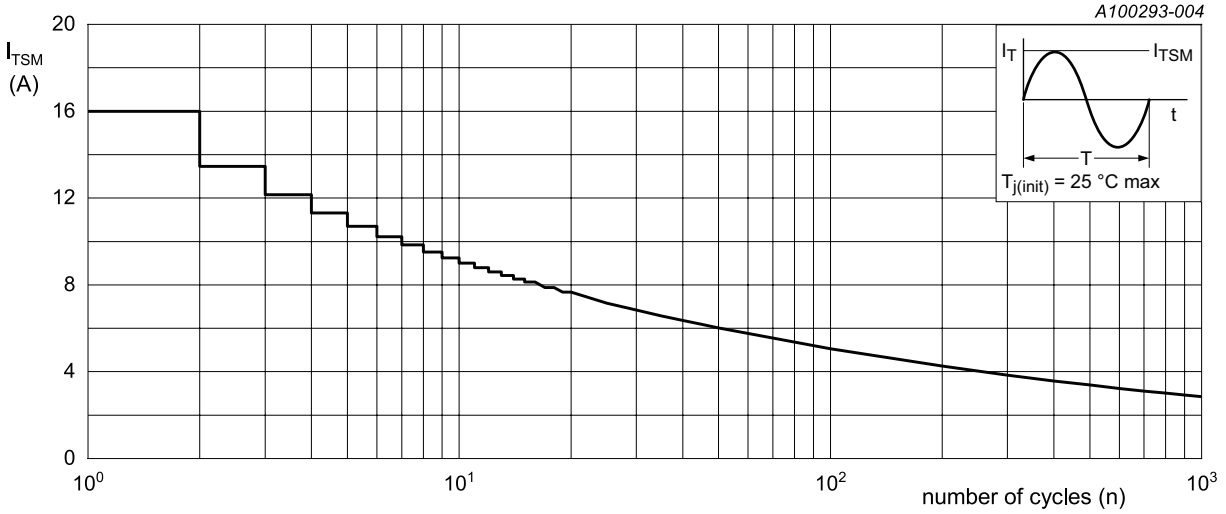


α = conduction angle

a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

Fig. 2. Total power dissipation as a function of RMS on-state current; maximum values



f = 50 Hz

Fig. 3. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

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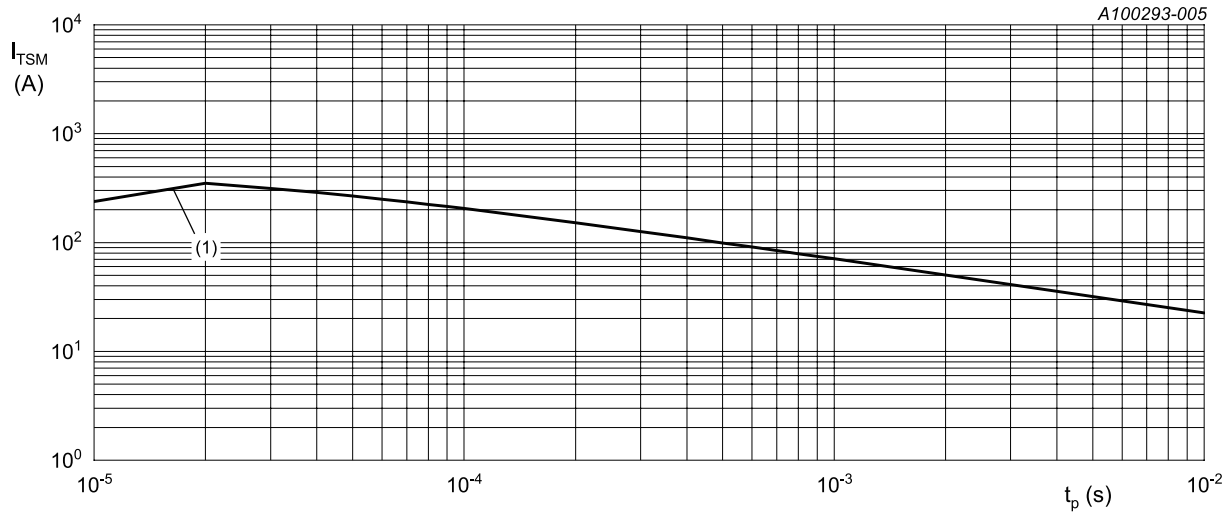

$t_p \leq 20$ ms

(1) dI_T/dt limit

Fig. 4. Non-repetitive peak on-state current as a function of pulse width; maximum values

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9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j\text{-}lead)}$	thermal resistance from junction to lead	full cycle; Fig. 5		-	40	-	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient free air	full cycle; printed circuit board: lead length = 4 mm		-	150	-	K/W

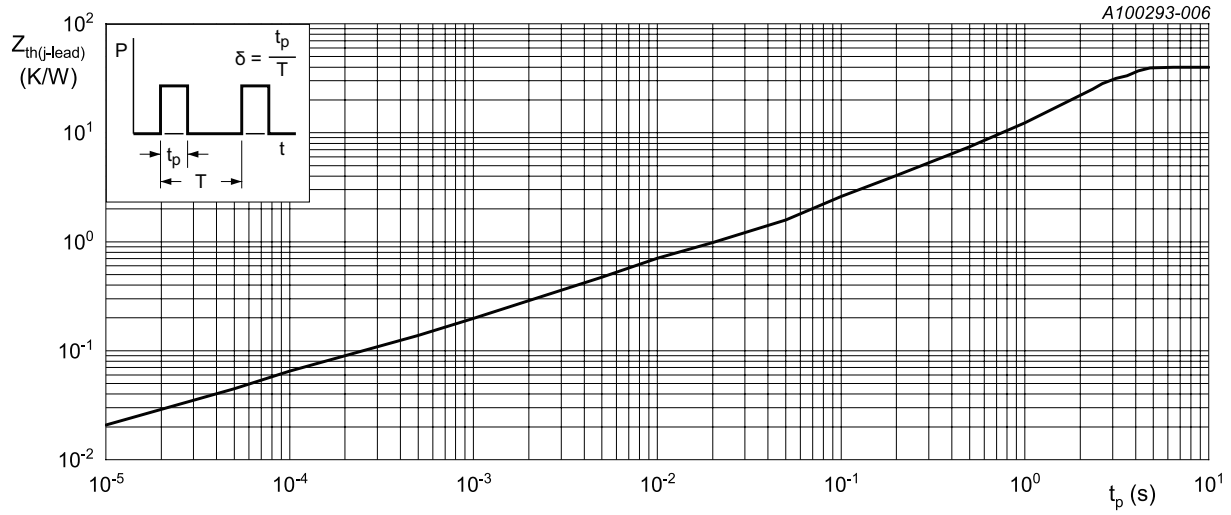

Fig. 5. Transient thermal impedance from junction to lead as a function of pulse width

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10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T2+ G+; T_j = 25 °C; Fig. 6		-	-	5	mA
		V_D = 12 V; I_T = 0.1 A; T2+ G-; T_j = 25 °C; Fig. 6		-	-	5	mA
		V_D = 12 V; I_T = 0.1 A; T2- G-; T_j = 25 °C; Fig. 6		-	-	5	mA
		V_D = 12 V; I_T = 0.1 A; T2- G+; T_j = 25 °C; Fig. 6		-	-	10	mA
I_L	latching current	V_D = 12 V; I_G = 0.1 A; T2+ G+; T_j = 25 °C; Fig. 7		-	-	10	mA
		V_D = 12 V; I_G = 0.1 A; T2+ G-; T_j = 25 °C; Fig. 7		-	-	20	mA
		V_D = 12 V; I_G = 0.1 A; T2- G-; T_j = 25 °C; Fig. 7		-	-	10	mA
		V_D = 12 V; I_G = 0.1 A; T2- G+; T_j = 25 °C; Fig. 7		-	-	10	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig.8		-	-	10	mA
V_T	on-state voltage	I_T = 2 A; T_j = 25 °C; Fig. 9		-	1.35	1.65	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 10		-	-	1	V
		V_D = 800 V; I_T = 0.1 A; T_j = 125 °C		0.2	-	-	V
I_D	off-state current	V_D = 800 V; T_j = 25 °C		-	-	10	µA
		V_D = 800 V; T_j = 125 °C		-	-	0.5	mA
I_R	reverse current	V_D = 800 V; T_j = 25 °C		-	-	10	µA
		V_D = 800 V; T_j = 125 °C		-	-	0.5	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 110 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 11		20	-	-	V/µs
dV_{com}/dt	rate of change of commutating voltage	V_D = 400 V; T_j = 110 °C; dI_{com}/dt = 0.44 A/ms; I_T = 1 A; gate open circuit		1	-	-	V/µs

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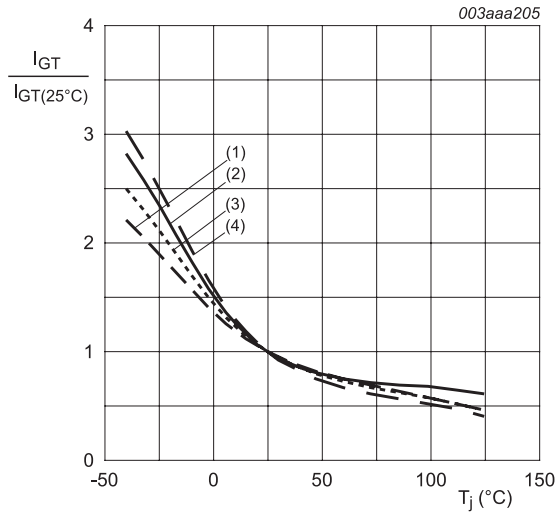


(1) T2- G+
(2) T2- G-
(3) T2+ G-
(4) T2+ G+

Fig. 6. Normalized gate trigger current as a function of junction temperature

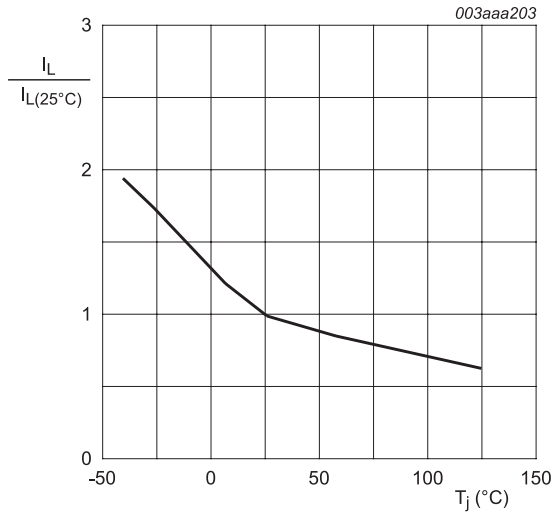


Fig. 7. Normalized latching current as a function of junction temperature

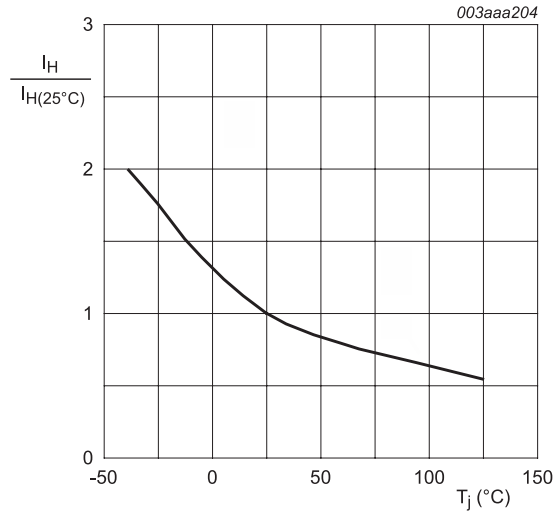
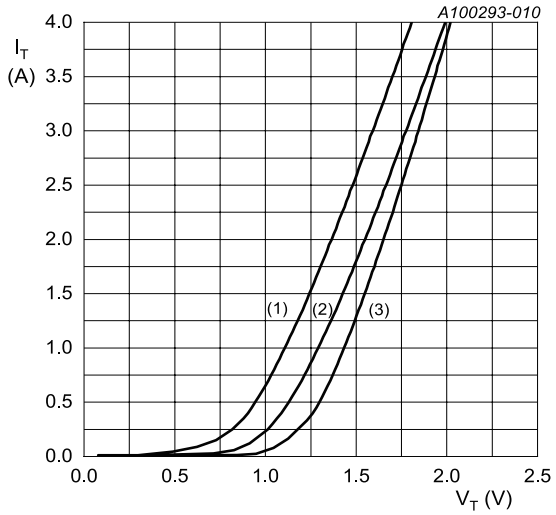


Fig. 8. Normalized holding current as a function of junction temperature



V_o = 1.12 V; R_s = 0.21 Ω
(1) T_j = 125 °C; typical values
(2) T_j = 125 °C; maximum values
(3) T_j = 25 °C; maximum values

Fig. 9. On-state current as a function of on-state voltage

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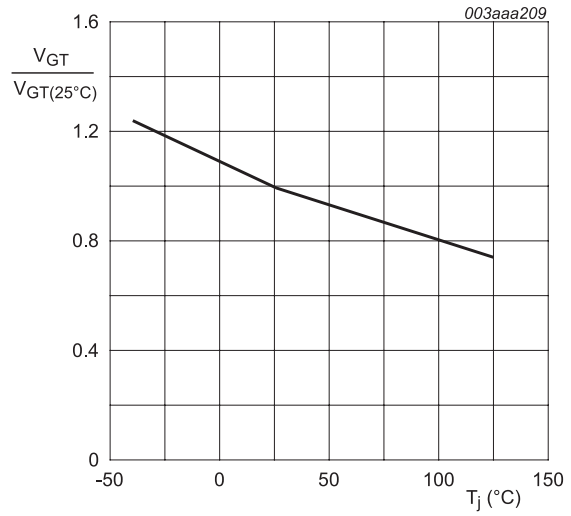
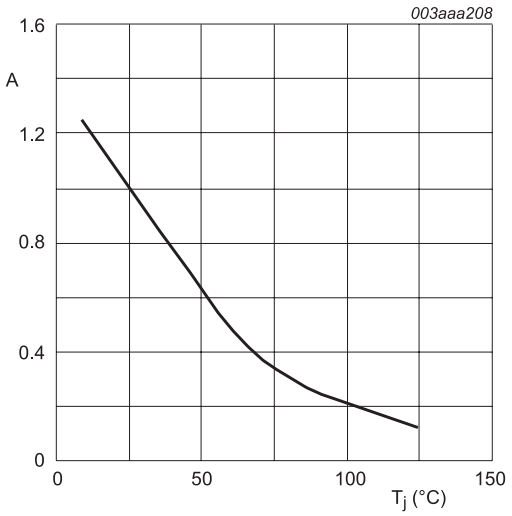


Fig. 10. Normalized gate trigger voltage as a function of junction temperature



$$A = \frac{dV_D(T_j\ °C)/dt}{dV_D(25°C)/dt}$$

Fig. 11. Normalized critical rate of rise of off-state voltage as a function of junction temperature; typical values

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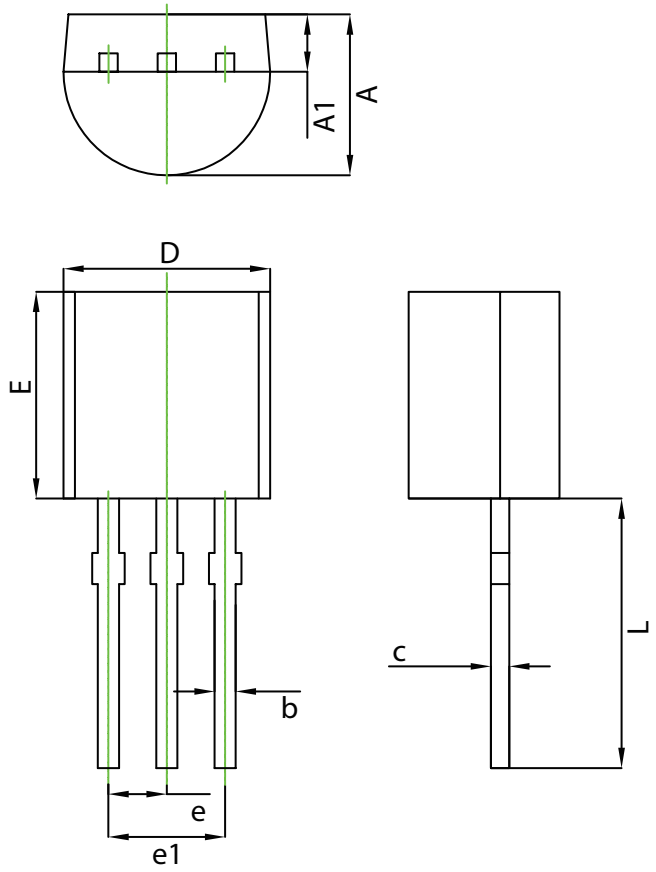
11. Package outline

Plastic single-ended leaded(through hole) package; 3 leads TO92



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.300	3.700	0.130	0.146
A1	1.100	1.400	0.043	0.055
b	0.380	0.550	0.015	0.022
c	0.360	0.510	0.014	0.020
D	4.300	4.700	0.169	0.185
E	4.300	4.700	0.169	0.185
e	1.270 TYP.		0.050 TYP.	
e1	2.440	2.640	0.096	0.104
L	14.100	14.500	0.555	0.571

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